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UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/637,165	08/08/2003	Marc Tremblay	SUN-P9324-SPL	2937

57960 7590 04/19/2007	EXAMINER	
SUN MICROSYSTEMS INC.	ZHE, MENG YAO	
C/O PARK, VAUGHAN & FLEMING LLP		
2820 FIFTH STREET	ART UNIT	PAPER NUMBER
DAVIS, CA 95618-7759	2109	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

	Application No.	Applicant(s)
	10/637,165	TREMBLAY ET AL.
Office Action Summary	Examiner	Art Unit	
	MengYao Zhe	2109	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>08 August 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 to 20* is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 to 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>08 August 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All   b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
　　Paper No(s)/Mail Date <u>1/29/07 9/5/06 8/6/04 4/14/06</u>.

4) ☐ Interview Summary (PTO-413)
　　Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

This is the initial Office Action based on the 10/637165 application filed on 8/8/2003.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on June 24, 2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS as to the merits.

Specification

The disclosure is objected to because of the following informalities:

Paragraphs 1 and 2 on page one are objected to because patent applications are mentioned without its application number.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 19 and 20 lack necessary physical articles or objects to constitute a machine or a manufacture within the meaning of 35 USC 101. They are clearly not a series of steps or acts to be a process nor are they a combination of chemical compounds to be a composition of matter. As such, they fail to fall within a statutory category. They are, at best, functional descriptive material *per se*.

Descriptive material can be characterized as either "functional descriptive material" or "non-functional descriptive material." Both types of "descriptive material" are non-statutory when claimed as descriptive material *per se*, 33 F.3d at 1360, 31 USPQ2d at 1759. When <u>functional</u> descriptive material is recorded on some computer-readable medium, it becomes structurally and functionally interrelated to the medium and will be statutory in most cases since use of technology permits the function of the descriptive material to be realized. Compare *In re Lowry*, 32 F.3d 1579, 1583-84, 32 USPQ2d 1031, 1035 (Fed. Cir. 1994)

Merely claiming non-functional descriptive material, i.e., abstract ideas, stored on a computer-readable medium, in a computer, or on an electromagnetic carrier signal, does not make it statutory. See *Diehr*, 450 U.S. at 185-86, 209 USPQ at 8 (noting that the claims for an algorithm in *Benson* were unpatentable as abstract ideas because "[t]he sole practical application of the algorithm was in connection with the programming of a general purpose computer.").

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form

the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 to 7, 9 to 16, and 18 to 20 are rejected under 35 U.S.C. 102(e) as being

anticipated by Rajwar et al. Patent No. 7,120,762, 10/10/2006 (hereafter Rajwar).

As per **claim 1**, Rajwar teaches **a method for executing a commit instruction to**

facilitate transactional execution on a processor, comprising:

> **encountering the commit instruction during execution of a program,**

> **wherein the commit instruction marks the end of a block of instructions to**

> **be executed transactionally;** *(Abstract and Column 9, lines 45 to 50: Rajwar*

> *discloses a system that predicts or speculate critical sections, and upon*

> *completion of the critical section, if no conflict results, the execution is committed,*

> *otherwise, it is squashed, meaning all execution is abandoned. Therefore, the*

> *instruction that performs the committing is considered to be the commit*

> *instruction.)*

and upon encountering the commit instruction, successfully completing

transactional execution of the block of instructions preceding the commit

instruction; *(Abstract and Column 9, lines 45 to 50)*

wherein changes made during the transactional execution are not

committed to the architectural state of the processor until the transactional

execution successfully completes. *(Abstract and Column 9, lines 45 to 50)*

As per **claim 10**, it claims for a computer system that contains all the instructions

capable of performing the method steps of claim 1. Since claim 1 is rejected, claim 10 is

rejected as well.

As per **claim 19**, it claims for a computing means, which contains all the means for

performing the method steps of claim 1. Since claims 1 is rejected, claim 19 is rejected

as well.

As per **claim 2**, Rajwar teaches **wherein successfully completing the transactional**

execution involves atomically committing changes made during the transactional

execution; and resuming normal non-transactional execution. *(Column 3, line 15)*

As per **claim 20**, it claims for a computing means, which contains all the means for

performing the method steps of claim 2. Since claims 2 is rejected, claim 20 is rejected

as well.

As per **claim 11**, it claims for a computer system that contains all the instructions

capable of performing the method steps of claim 2. Since claim 2 is rejected, claim 11 is

rejected as well.

As per **claim 3**, Rajwar teaches

> **wherein atomically committing changes made during the transactional**
>
> **execution involves: treating store-marked cache lines as locked, thereby**
>
> **causing other processes to wait to access the store-marked cache lines;**
>
> *(Column 5, lines 30 to 40, Column 6, lines 55 to end, and Column 7, first 4 lines:*
>
> *The STORE instruction usually follows the LOCK instruction, making all other*
>
> *threads break out of their parallel execution and are serialized while waiting for*
>
> *the LCOK to be release.)*
>
>
> **clearing load marks from cache lines; committing store buffer entries**
>
> **generated during transactional execution to memory, wherein committing**
>
> **each store buffer entry involves unmarking, and thereby unlocking, a**
>
> **corresponding store-marked cache line;** *(Column 8, lines 40 to 50; Column 8,*
>
> *lines 53 to 60: Any writes onto the cache by another thread that does not have*

the lock causes invalidation of cache, part of the standard cache protocol. This is

used to detect conflicts during the execution of Critical section. It is inherent in

the Teachings of Rajwar that specific steps of clearing and unmarking marks is

part of the standard cache protocol. Thus whenever a commit is performed, or

even when another attempt is tried, the cache is flushed, thus clearing all

previous marks.)

and committing register file changes made during transactional execution.
(last paragraph in Column 5: The system commits to all changes made during

the critical section, which include the read/modify/write instructions. When

modify/write are executed, they change the content of registers.)

As per **claim 12**, it claims for a computer system that contains all the instructions

capable of performing the method steps of claim 3. Since claim 3 is rejected, claim 12 is

rejected as well.

As per **claim 4**, Rajwar teaches

wherein if an interfering data access from another process is encountered

during the transactional execution and prior to encountering the commit

instruction, the method further comprises: discarding changes made

during the transactional execution; and attempting to re-execute the block

of instructions. *(Column 8, lines 50 to 65: If conflict occurs, all execution or*

changes are abandoned, and the system tries to execute again if the number of

reties have not exceeded the limit.)

As per **claim 13**, it claims for a computer system that contains all the instructions

capable of performing the method steps of claim 4. Since claim 4 is rejected, claim 13 is

rejected as well.

As per **claim 5**, Rajwar teaches

> **wherein for a variation of the commit instruction, successfully completing**
>
> **the transactional execution involves: atomically committing changes made**
>
> **during the transactional execution; and commencing transactional**
>
> **execution of the block of instructions following the commit instruction.**
> *(Abstract and Column 9, lines 45 to 50, Column 3, line 15)*

As per **claim 14**, it claims for a computer system that contains all the instructions

capable of performing the method steps of claim 5. Since claim 5 is rejected, claim 14 is

rejected as well.

As per **claim 6**, Rajwar teaches

> **wherein potentially interfering data accesses from other processes are**
>
> **allowed to proceed during the transactional execution of the block of**

instructions. *(Column 2, lines 47 to 50: the purpose of the entire invention as disclosed by Rajwar is to allow multiple threads running during a critical section.)*

As per **claim 15**, it claims for a computer system that contains all the instructions capable of performing the method steps of claim 6. Since claim 6 is rejected, claim 15 is rejected as well.

As per **claim 7**, Rajwar teaches **wherein the block of instructions to be executed transactionally comprises a critical section** *(Column 2, lines 47 to 50)*

As per **claim 16**, it claims for a computer system that contains all the instructions capable of performing the method steps of claim 7. Since claim 7 is rejected, claim 16 is rejected as well.

As per **claim 9**, Rajwar teaches **wherein the commit instruction is defined in a platform-independent programming language** *(Column 10, lines 8 to 15: Rajwar's invention is applicable to a wide range of different computer architectures. Since his invention can only be accomplished by programming language, it is therefore platform independent.)*

As per **claim 18**, it claims for a computer system that contains all the instructions

capable of performing the method steps of claim 9. Since claim 9 is rejected, claim 18 is

rejected as well.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness

under 35 U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating
       obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the

various claims was commonly owned at the time any inventions covered therein were

made absent any evidence to the contrary. Applicant is advised of the obligation under

37 CFR 1.56 to point out the inventor and invention dates of each claim that was not

commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g)

prior art under 35 U.S.C. 103(a).

Claims 8 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Rajwar et al. Patent No. 7,120,762, 10/10/2006, (hereafter Rajwar), in view of Hecht et

al, Pub. No. US 2003/0064808 (hereafter Hecht).

As per **claim 8**, Rajwar teaches

> **all of claim 1 and that the invention as he disclosed may be used on**
>
> **different computer architecture, meaning that they can be platform**
>
> **independent** *(Column 10, lines 8 to 15)*

Rajwar does not teach the commit instruction being platform dependent.

However, Hecht teaches a

> **converter program that converts platform independent programs into**
>
> **platform dependent programs** for the purpose of running the program on a
>
> specific type of machine *(Paragraph 14)*

It would have been obvious to one having ordinary skill in the art at the time of the

invention to have modified the invention of Rajwar witth

> **Converting the platform independent instruction to platform dependent**
>
> **instruction,**

as taught by Hecht, because it allows the program to run on a specific type of machine.

As per **claim 17**, it claims for a computer system that contains all the instructions

capable of performing the method steps of claim 8. Since claim 8 is rejected, claim 17 is

rejected as well.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to MengYao Zhe whose telephone number is 571-272-

6946. The examiner can normally be reached on Monday Through Friday, 7:30 - 5:00

EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Joseph Del Sole can be reached on 571-272-1130. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

M.Z.

JOSEPH DEL SOLE
SUPERVISORY PATENT EXAMINER

4/16/07